Neeta Pandey

Electronics and Communication Engineering

Email: neetapandey@dce.ac.in

Qualifications

M. E. (Microelectronics) Ph. D.

Areas of Interest

Analog and Digital VLSI Design, Current mode ADC Design

Summary

Motivated **Teaching Professional** with approximately 31 years teaching and research experience in Electronics and Communication Engineering. Accomplished lecturer who effectively articulates information and responds honestly to questions from students.

Highlights

- Inspiring teacher with Effective Communication
- Uphold high morale and ethics of this noble profession

Subjects Taught

- VLSI Design
- Deep Submicron VLSI Design
- Basic and Advanced courses in Digital Electronics
- Computer Architecture
- Analog Filter design
- Analog Integrated Circuits

Honours, awards and recognitions acquired by faculty

- Member Editorial Board - AEU Int. J. Electronics and Communication, Advances in Electrical and Electronics Engineering
- Excellence in research Award from Delhi Technological University Delhi for research papers published in year 2018, 2019 and 2020
- Outstanding Branch Counsellor award from IEEE USA 2008 and cash prize of US $500.
- Outstanding Branch Counsellor award from IEEE Delhi Section 2008.
- Inclusion in Marquis Who's who 2010
- National Scholarship for class 10

- Designated reviewer for International Journals published by Weily, IEEE, IET, Taylor and Francis, Springer and Elsevier.

- Technical Program Chair for IEEE conference on Signal Processing, VLSI and Communication Engineering, 2019

- Designated reviewer for International Conferences

- Member of Technical Program Committee of International Conferences

- Member of professional societies such as IEEE, Women in Engineering (WIE), an affinity group of IEEE, ISTE.

- Technical Program Chair for IEEE conference on Signal Processing, VLSI and Communication Engineering

Accomplishment

- Contributing author to 148 review publications in various international journals and 115 international conferences.

- Co-authored books
  - Model and Design of Improved Current Mode Logic Gates, Springer 2020
  - IC Analog Filter, LAP Lambert Academic Publishing, 2011, ISBN 978-3-8433-6007-4
  - Wave Filter: A Wave Active Equivalence Design Approach LAP Lambert Academic Publishing, 2011, ISBN 978-3844381696, 2011
  - Realization of analog controllers using OTRA, LAP Lambert Academic Publisher, West Germany, 2012, ISBN no. 978-3-659-16439-2
  - Dynamic Current Mode Logic: Concepts to Advancements, LAP LAMBERT Academic Publishing, 2021, ISBN-13: 978-620-4-20810-7

- Co-authored book chapter
  - N. Pandey, R. Pandey, R Verma, Higher-order fractional elements: realizations and applications, Fractional-Order Design: Devices, Circuits, Systems, 403, 2021 Elsevier

- **Awards/ Recognition**
  - Outstanding Branch counsellor award from IEEE USA 2008 and cash prize of US $500.
  - Outstanding Branch Counsellor award from IEEE Delhi Section 2008
  - Inclusion in Marquis Who's who 2010
  - Participated in IUCEE, Project GENTLE (Global Education Network for Teaching and Learning Engineering), in collaboration with Inpods Oct.2014. Received a letter of appreciation and cash prize.
  - Best paper Award for "OTRA based shadow filters" in IEEE India Conference (INDICON), Dec 2015**.**
  - Commendable Research Excellence Award in 2018,2019 and 2020.
  - Listed in 2% scientist by Stanford.

Memberships

- Member of professional societies such as IEEE (Senior Member), Women in Engineering (WIE), an affinity group of IEEE, ISTE.

Publications:

Journal Paper

In press

1. D Singh, K. Gupta, N. Pandey, A Novel Low-Power Nonvolatile 8T1M SRAM Cell, Arabian Journal for Science and Engineering, 1-17, online 1/9/2021 (SCI – 2.334)
2. K Suneja, N. Pandey, R. Pandey, Systematic Realization of CFOA Based Rössler Chaotic System and Its Applications. Arabian Journal for Science and Engineering, 1-17, online 17/1/2022 (SCI – 2.334)
3.

Published

1. S. Singh, S. Jain, R. Pandey, N. Pandey Adaptive biased current differencing trans-conductance amplifier, AEU - International Journal of Electronics and Communications, 128, 153494, Jan 2021. **(SCI – 3.183)**
2. M. Gupta, K. Gupta, N. Pandey A data-independent 9T SRAM cell with enhanced ION/IOFF ratio and RBL voltage swing in near threshold and sub-threshold region, International Journal of Circuit Theory and Applications, 49, 4, Apr 2021, 953-969. **(SCI – 2.038)**
3. M. Gupta, K. Gupta, N. Pandey, Comparative Analysis of the Design Techniques for Low Leakage SRAMs at 32nm, Microprocessors and Microsystems, 85, 2021. **(SCI – 1.525)**
4. M. Gupta, K. Gupta,N. Pandey, A novel PVT-variation-tolerant Schmitt-trigger-based 12T SRAM cell with improved write ability and high ION/IOFF ratio in sub-threshold region, International Journal of Circuit Theory and Applications, 49, 11, November 2021Pages 3789-3810 **(SCI – 2.038)**
5. S Gupta, N. Pandey, RS Gupta, Analytical modeling of dual-metal gate stack engineered junctionless accumulation-mode cylindrical surrounding gate (DMGSE-JAM-CSG) MOSFET, Appl. Phys. A, 127, 2021, 520. **(SCI – 2.584)**
6. S. Gupta, N. Pandey, RS Gupta, Temperature dependency and linearity assessment of dual-metal gate stack junctionless accumulation-mode cylindrical surrounding gate (DMGS-JAM-CSG) MOSFET, Physica Scripta 96 (12), 124055 **(SCI – 2.487)**
7. N. Kumar, M. Kumar, N. Pandey, Unified floating immittance emulator based on CCTA, Microelectronics Journal 118, 105289, 2021 **(SCI – 1.605)**
8. R. Arundeepakvel, Jatin, P. Khatter, N. Pandey, Shahram Minaei, A novel design for voltage inverting metamutator and its applications, Microelectronics Journal, 113, 2021. **(SCI – 1.605)**
9. N. Yadav, N. Pandey, D. Nand, Leakage reduction in dual mode logic through gated leakage transistors, Microprocessors and Microsystems, 84, 2021. **(SCI – 1.525)**
10. A. S. Kumar, S. Jain, N. Pandey, Clock Aligned Input Adiabatic Logic, Microelectronics Journal, 114, 105122, 2021. **(SCI – 1.605)**
11. R. Sivaram, K. Gupta & N. Pandey, Impact of multi threshold transistor in positive feedback source coupled logic (PFSCL) fundamental cell, Analog Integrated Circuits and Signal Processing, 109, 173-185, 2021. **(SCI – 1.337)**
12. G. Varshney, N. Pandey, R. Pandey, Electronically Tunable Multifunction Transadmittance-Mode Fractional-Order Filter, Arabian Journal for Science and Engineering, 46, 1067–1078, 2021. **(SCI – 2.334)**
13. G .Varshney, N. Pandey, R. Pandey, Electronically tunable fractional-order multivibrator using OTA and its application as versatile modulator, AEU-International Journal of Electronics and Communications 141, 153956, 2021 **(SCI – 3.183)**
14. G. Varshney, N. Pandey, R. Pandey, Generalization of shadow filters in fractional domain, International Journal of Circuit Theory and Applications, 49, 10, October 2021,Pages 3248-3265 **(SCI – 2.038)**
15. P. Kumar, N. Pandey, SK Paul, Electronically Tunable VDTA-Based Multi-function Inverse Filter, Iranian Journal of Science and Technology, Mar 2021. **(SCI – 1.194)**

16. O. K. Gupta, N. Pandey M. Gupta, Improved reversed nested miller frequency compensation techniques using flipped and folded flipped voltage follower with resistor for three stage amplifier AEU - International Journal of Electronics and Communications, 142, 154004, 2021. **(SCI – 3.183)**
17. C. Parashar, A. Kumar Trivedi, A. Agarwal, N. Pandey, Footer Voltage Controlled Dual Keeper Domino Logic with Static Switching Approach, Advances in Electrical and Electronic Engineering, 18, 4, 255-263, 2020. **Scopus**
18. R. Jain, K. Gupta, N. Pandey, Hybrid Dynamic CML with Modified Current Source (H-MDyCML): A Low-Power Dynamic MCML Style, Advances in Electrical and Electronic Engineering, 19, 1, 57-65, 2021. **Scopus**
19. R Jain, K Pahwa, N. Pandey, Booth-Encoded Karatsuba: A Novel Hardware-Efficient Multiplier, Advances in Electrical and Electronic Engineering 19 (3), 272-281, 2021. **Scopus**
20. M. Bhardwaj, S. Pandey, N. Pandey, A Novel Design of High-Performance Low Power Phase-Frequency Detector for CMOS PLL Frequency Synthesizer, International Journal of Sensors Wireless Communications and Control, 10, 6, 2020, 838-845. **Scopus**
21. S Singh, Jatin, N. Pandey, R. Pandey, Electronically Tunable Grounded Capacitance Multiplier, IETE Journal of Research, 1-12, 2020 **(SCI - 2.333)**
22. N. Pandey, R. Pandey, R Anurag, R Vijay, A Class of Differentiator-Based Multifunction Biquad Filters Using OTRAs, Advances in Electrical and Electronic Engineering 18 (1), 31-40, 2020 **Scopus**
23. P Sharma, S Gupta, K. Gupta, N. Pandey, A low power subthreshold Schmitt Trigger based 12T SRAM bit cell with process-variation-tolerant write-ability, Microelectronics J., 97, 104703, 2020 **(SCI – 1.605)**
24. G. Komanapalli, R. Pandey, N. Pandey New Electronically tunable low-frequency quadrature oscillator using operational transresistance amplifier, IETE Journal of Research, 1-9, 2020 **(SCI - 2.333)**
25. S Jain, N. Pandey, Single Clock Diode Based Adiabatic Logic Family at Sub-90nm Regime, Advances in Electronics Engineering, 245-259, 2020
26. R. Jain, N. Pandey, Realization of Various Topologies of Adders Based on H-DyCML, International Journal of Innovative Technology and Exploring Engineering (IJITEE), 9, 1885-1191 2020
27. V. Bhanoo, A. Gangal, N.Pandey, Subthreshold Low-Transconductance M-CDTA based Low Frequency Current Mode Universal Filter, International Journal of Engineering Trends and Technology, 68(5), 16-22, 2020
28. R. Singh, N. Pandey, A Low Power and Area Efficient Design of Dadda Multiplier by exploring 4:2 Compressors and Brent Kung Adder, International Journal of Advanced Science and Technology, 29, 10044-10054, 2020.
29. P. Kumar, N. Pandey, S. K. Paul, Realization of Resistorless and Electronically Tunable Inverse Filters Using VDTA, Journal of Circuits, Systems and Computers 28 (09), 1950143, 2019
30. G. Komanapalli, R. Pandey, N. Pandey, Operational Transresistance Amplifier Based Wienbridge Oscillator and Its Harmonic Analysis, Wireless Personal Communications 108 (1), 1-17, 2019
32. E. Yuce, R. Verma, N. Pandey, S. Minaei, New CFOA-based first-order all-pass flters and their applications. AEU - International Journal of Electronics and Communications, 103, 57-63, 2019. **(SCI – 3.183)**
33. S. Gupta, K. Gupta, B. H. Calhoun, N. Pandey, Low-Power Near-Threshold 10T SRAM Bit Cells With Enhanced Data-Independent Read Port Leakage for Array Augmentation in 32-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 66(3), 978–988, 2019. **(SCI-3.605)**
34. M. Gupta, K. Gupta, N. Pandey. A design of low leakage cache memory cell for high performance processors. Journal of Information and Optimization Sciences 40 (2), 279-290, 2019
35. R. Verma, N. Pandey, R. Pandey. CFOA based low pass and high pass fractional step filter realizations. AEU-International Journal of Electronics and Communications 99, 161-176, 2019 **(SCI – 3.183)**
36. P Bajpai, N. Pandey, K. Gupta, J Panda, LECTOR incorporated differential cascode voltage swing logic (L-DCVSL), Analog Integrated Circuit and Signal Processing 100 (1), 221-234, 2019 **(SCI – 1.337)**
37. M. Tiwari, N. Pandey, SK Paul, M. Rizvi. Programmable CCCII: Reliability Analysis and Design Methodology. IET Circuits, Devices & Systems, 13, 4, 487-493, July 2019. **(SCI – 1.297)**
38. G. Komanapalli, R. Pandey, N. Pandey. New sinusoidal oscillator configurations using operational transresistance amplifier. International Journal of Circuit Theory and Applications, 47, 5 Pages 666-685 May 2019 **(SCI – 2.038)**

39. A Mann, N Malhotra, N. Pandey Adaption of Power Gating in Positive Feedback Adiabatic Logic Circuits, International Journal of Advance Research and Innovation, 7 (3), 281-284, 2019

40. A Jain, N. Pandey, P Jain. FPGA-Based Architecture for Implementation of Discrete Sine Transform. Advances in System Optimization and Control, 13-22, 2019

41. P. Pahalwan, P. Tripathi, P. Gola, N. Pandey, D Nand, Programmable Gain Amplifier Using Operational Floating Current Conveyors, AEU-International Journal of Electronics and Communications, 90, 163-170, 2018. **(SCI – 3.183)**

42. S. Gupta, K. Gupta, N. Pandey, Pentavariate Vmin Analysis of a Subthreshold 10T SRAM Bit Cell With Variation Tolerant Write and Divided Bit-Line Read IEEE Transactions on Circuits and Systems I: 65, 10, 3326 – 3337,2018. **(SCI-3.605)**

43. V. Bhatnagar, P. Kumar, N. Pandey, S Pandey, A dual V t disturb-free subthreshold SRAM with write-assist and read isolation, Journal of Semiconductors 39 (2), 025002, 2018. **Scopus**

44. V. Bhatnagar, P. Kumar, N. Pandey, S Pandey, A boosted negative bit-line SRAM with write-assisted cell in 45 nm CMOS technology Journal of Semiconductors 39 (2), 025001, 2018 **Scopus**

45. S. Oruganti, N. Pandey, R. Pandey, Electronically tunable high gain current-mode instrumentation amplifier, AEU-International Journal of Electronics and Communications 95, 16-23, 2018 **(SCI – 3.183)**

46. R Verma, N. Pandey, R. Pandey, Realization of a higher fractional order element based on novel OTA based IIMC and its application in filter, Analog Integrated Circuits and Signal Processing, 97 (1), 177-191, 2018. **(SCI – 1.337)**

47. G. Komanapalli, N. Pandey, R. Pandey, New realization of third order sinusoidal oscillator using single OTRA, AEU-International Journal of Electronics and Communications 93, 182-190, 2018 **(SCI – 3.183)**

48. S. Oruganti, Y Gilhotra, N. Pandey, R. Pandey, OTRA Based Piece-Wise Linear VTC Generators and Their Application in High-Frequency Sinusoid Generation, Advances in Electrical and Electronic Engineering 15 (5), 806-814, 2018 **Scopus**

49. D Nand, N. Pandey, New Configuration for OFCC-Based CM SIMO Filter and its Application as Shadow Filter, Arabian Journal for Science and Engineering, 1-12, 2018 **(SCI-2.334)**

50. N. Pandey, B. Choudhary, K. Gupta, A Mittal, New Sleep-Based PFSCL Tri-State Inverter/Buffer Topologies, Journal of Circuits, Systems and Computers, 1750186, 2017

51. R. Verma, N. Pandey, R. Pandey, Electronically Tunable Fractional Order Filter, Arabian Journal for Science and Engineering, 1-14, 2017 **(SCI-2.334)**

52. N. Pandey, V. Kumar, A. Goel, A. Gupta, Electronically tunable LC high pass ladder filter using OTRA, 10.21917/ijme.2017.0079, 2017

53. S. Gupta, K. Gupta, N. Pandey, A 32-nm Subthreshold 7T SRAM Bit Cell With Read Assist, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 25 12, 3473-3483, 2017 (**SCI-2.312)**

54. L. Safari, N. Pandey, N Herencsar, F Khateb, Special Issue on Current-Mode Circuits and Systems; Recent Advances, Design and Applications, AEU-International Journal of Electronics and Communications, 2017 **(SCI – 3.183)**

55. K. Gupta, N. Pandey, M. Gupta, Dynamic positive feedback source-coupled logic (D-PFSCL) International Journal of Electronics 103 (10), 1626-1638, 2016 **(SCI – 1.336)**

56. N. Pandey, K. Gupta, B. Choudhary, New Proposal for MCML Based Three-Input Logic Implementation, VLSI Design 2016 Article ID 8712768

57. P. Bajpai, N. Pandey, K. Gupta, S Bagga, J Panda, On Improving the Performance of Dynamic DCVSL Circuits, Journal of Electrical and Computer Engineering 2017 Article ID 8207104

58. V. Bhatia, N. Pandey, Modified Tang and Pun's Current Comparator and Its Application to Full Flash and Two-Step Flash Current Mode ADCs, Journal of Electrical and Computer Engineering 2017 Article ID 8245181

59. G. Komanaplli, N. Pandey, R. Pandey New Realization of Quadrature Oscillator using OTRA International Journal of Electrical and Computer Engineering (IJECE) vol. 7, No. 1815-1823 Aug 2017

60. R. Verma, N. Pandey, R. Pandey, Electronically Tunable Fractional Order All Pass Filter, IOP Conference Series: Materials Science and Engineering 225 (1), 012229, 2017

61. P. Gupta, R. Pandey, N. Pandey, Voltage Mode Single CDBA Based Multifunction Filter IOP Conference Series: Materials Science and Engineering 225 (1), 012243, 2017

62. G. Komanapalli, N. Pandey, R. Pandey, Single OTRA Based Low Frequency Sinusoidal Oscillator Realization, IOP Conference Series: Materials Science and Engineering 225 (1), 012151, 2017

63. D. Nand, N. Pandey, Transadmittance Mode First Order LP/HP/AP Filter and its Application as an Oscillator, IOP Conference Series: Materials Science and Engineering 225 (1), 012150, 2017

64. D. Nand, N. Pandey, A New Proposal for OFCC-based Instrumentation Amplifier, International Journal of Electrical and Computer Engineering 7 (1), 134, 2017

65. N. Pandey, G Varshney, R. Pandey, Differential Voltage Current Conveyor Realization based on CMOS Inverters, i-Manager's Journal on Electronics Engineering 7 (2), 14,2016

66. N. Pandey, R. Pandey, N. Sabharwal, Realization of Diode-Free OTRA based Time Marker Generator, i-Manager's Journal on Electronics Engineering 7 (1), 16, 2016

67. K. Gupta, P Gupta, R. Pandey, N. Pandey CDBA -Current Based Instrumentation Amplifier, Journal of Communications Technology, Electronic s and Computer Science, 4, 2016

68. Nitish, N. Pandey, K. Gupta, M K Saini, DFAL based flexible multi-modulo prescaler, ICTACT Journal on Microelectronics, 273-280, 2016

69. N. Saxena, S Dutta, N. Pandey, An Efficient Hybrid PFSCL based Implementation of Asynchronous Pipeline, i-Manager's Journal on Circuits & Systems 4 (3), 6 - 14, 2016

70. N. Pandey, K. Gupta, G Bhatia, B. Choudhary, MOS Current Mode Logic Exclusive-OR Gate using Multi-Threshold Triple-Tail Cells, Microelectronics Journal. 57, 13–20, 2016 **(SCI – 1.605)**

71. N. Pandey, K. Gupta, B. Choudhary, New proposal for MCML based three input logic implementation, VLSI Design, 2016, Article ID 8712768, 10 pages

72. R. Pandey, N. Pandey, N Singhal, Single VDTA Based Dual Mode Single Input Multi output Biquad Filter, Journal of Engineering, 2016, Article ID 1674343, 10 pages,

73. D. Nand, N. Pandey, A new proposal for OFCC based Instrumentation Amplifier, International Journal of Electrical and Computer Engineering, 7, 1,31 – 39, 2016**. (SCIE-4.360)**

74. S. Kumari, S Gupta, N. Pandey, R. Pandey, R Anurag, LC-ladder filter systematic implementation by OTRA, International Journal Engineering Science and Technology, 19, 4, 1808-1814, 2016

75. P. Kumar, N. Pandey, S K Paul, Operational Simulation of LC Ladder Filter Using VDTA, Active and Passive Electronic Components, 2017, Article ID 1836727, 8 pages **Scopus**

76. V. Bhatia, N. Pandey, Modified Tang's Current Comparator and Its Application to Full Flash and Two-Step Flash Current Mode ADCs, Journal of Electrical and Computer Engineering, 2017, Article ID 8245181, 12 pages

77. N. Pandey, D Nand, R. Pandey, Generalised operational floating current conveyor based instrumentation amplifier, IET Circuits, Devices & Systems 10 (3), 209-219,2016 **(SCI – 1.297)**

78. N. Pandey, D Nand, VV Kumar, VK Ahalawat, C Malhotra Realization of OFCC based Transimpedance Mode Instrumentation Amplifier, Advances in Electrical and Electronic Engineering 14 (2), 162-167, 2016 **Scopus**

79. N. Pandey, D Garg, K. Gupta, B. Choudhary, Hybrid Dynamic MCML Style: A High Speed Dynamic MCML Style, Journal of Engineering, 2016 (2016), Article ID 8027150, 10 pages

80. N. Pandey, A Mittal, B. Choudhary, K. Gupta, Bus Implementation using New Low Power PFSCL Tri-state buffers, Active and Passive Electronic Components 2017 Article ID 8245181 **Scopus**

81. K. Gupta, N. Pandey, M. Gupta, Dynamic Positive-Feedback Source-Coupled Logic (D-PFSCL), International Journal of Electronics, 103, 10, 1626-1638, 2016 **(SCI – 1.336)**

82. N. Pandey, R. Pandey, Approach for third order quadrature oscillator realisation, IET Circuits, Devices & Systems 9 (3), 161-171, 2015. **(SCI – 1.297)**

83. N. Pandey, P. Kumar, S. K Paul, Voltage differencing transconductance amplifier based resistorless and electronically tunable wave active filter, Analog Integrated Circuits and Signal Processing, 84, pages107–117 (2015) **(SCI – 1.337)**

84. N. Pandey, B. Choudhary, Improved tri-state buffer in MOS current mode logic and its application, Analog Integrated Circuits and Signal Processing, 84, 2, 333-340, 2015 **(SCI – 1.337)**

85. R. Pal, R. Pandey, N. Pandey, Ramesh Chandra Tiwari, Single CDBA Based Voltage Mode Bistable Multivibrator and Its Applications, Circuits and Systems 6 (11), 237

86. R. Pandey, N. Pandey, Surabh Chittranshi, S. K Paul, Operational Transresistance Amplifier Based PID Controller, Advances in Electrical and Electronic Engineering 13 (2), 171-181, 2015. **Scopus**

87. N. Pandey, K. Gupta, M. Gupta, An efficient triple-tail cell based PFSCL, Microelectronics Journal, 1001-1007, 2014. **(SCI – 1.605)**

88. N. Pandey, D. Nand, Z. Khan, Operational floating current conveyor-based single-input multiple-output transadmittance mode filter, Arabian Journal for Science and Engineering 39, 7991–8000, 2014. **(SCI-2.334)**

89. R. Pandey, N. Pandey, R. Mullick, S. Yadav and R. Anurag, All Pass Network based MSO using OTRA, Advances in Electronics, 2015, Article ID 382360, 7 pages

90. R. Sridhar, N. Pandey, A. Bhattacharyya, V. Bhatia, High Speed High Resolution Current Comparator and its Application to Analog to Digital Converter, J. Inst. Eng. India Ser. B, **97**, pages147–154, 2016.

91. R. Pandey, N. Pandey, G. Komanapalli, R. Anurag, OTRA Based Voltage Mode Third Order Quadrature Oscillator, ISRN Electronics, 2014 , Article ID 126471, 5 pages

92. N. Pandey, R. Pandey, R. Sridhar, V. Bhatia, A. K. Singh, P. Kumar, CDTA based current mode ADC, International Journal of Advance Research In Science And Engineering http://www.ijarse.com IJARSE, 3, Special Issue (01), 499 -505, 2014

93. A. Tayal, N. Pandey, R. Pandey, Residue adder based high speed 8-bit Vedic multiplier, International Journal of Electrical and Electronics Engineers No.6, 158 – 162, 2014. **Scopus**

94. N. Pandey, K. Gupta, R. Pandey, R. Pandey, T. Mittal, Novel oscillators in subthreshold regime, International Journal of Electrical and Electronics Engineers, 6, 151 – 156, 2014. **Scopus**

95. N. Singhal, R. Pandey, N. Pandey, Dual mode biquadratic filter using single VDTA, International Journal of Electrical and Electronics Engineers, 6, 134 – 139, 2014. **Scopus**

96. K. Gupta, N. Pandey, M. Gupta, Analysis and design of MOS current mode logic exclusive-OR gate using triple-tail cells, Microelectronics Journal, 44, 6, 561–567, 2013. **(SCI – 1.605)**

97. K. Gupta, N. Pandey, M. Gupta, Low-Voltage MOS Current Mode Logic Multiplexer, Radioengineering, 259-268, 2013. **(SCI – 0.925)**

98. K. Gupta, N. Pandey, M. Gupta, MCML D-Latch Using Triple-Tail Cells: Analysis and Design, Active and Passive Electronic Components, 2013, Article ID 217674, 9 pages **Scopus**

99. M. Bothra, R. Pandey, N. Pandey, S. K. Paul, Operational Trans-Resistance Amplifier Based Tunable Wave Active Filter, Radioengineering, 22, 159 -166, 2013 **(SCI – 0.925)**

100. N. Pandey, S. K. Paul, Mixed mode universal filter, J Circuit Syst. Comp., 22, 1, 1250064, 2013.

101. N. Pandey, P. Kumar, J. Choudhary, Current Controlled Differential Difference Current Conveyor Transconductance Amplifier and Its Application as Wave Active Filter, ISRN Electronics, 2013. Article ID 968749, 11 pages

102. N. Pandey, S. Arora, R. Takkar, R. Pandey, DVCCCTA-Based Implementation of Mutually Coupled Circuit, ISRN Electronics, 2012. Article ID 303191, 6 pages

103. N. Pandey, R. Pandey, Current Mode Full-Wave Rectifier Based on a Single MZC-CDTA Active and Passive Electronic Components, 2013 Article ID 967057, 5 pages **Scopus**

104. N. Pandey, D. Nand, Z. Khan, Single-Input Four-Output Current Mode Filter Using Operational Floating Current Conveyor, Active and Passive Electronic Components, 2013, Article ID 318560, 8 pages **Scopus**

105. N. Pandey, S. Sayal, M. Tripathi, R. Pandey, Realization of S-G Shapers for Detector Readout Front Ends, Elixir Signal Processing 66, 20690-20699, 2014

106. N. Pandey, V. Bhatia, A. Bhattacharyya, A reference generating inverter-switching-threshold- voltage based current comparator, Journal of Electron Devices, 14, 1100-1103, 2012.

107. N. Pandey, R. Pandey, S. K. Paul A first order all pass filter and its application in a quadrature oscillator, Journal of Electron Devices, 12, 772-777, 2012.

108. R. Sridhar, N. Pandey, V. Bhatia, A. Bhattacharyya, New realization of current comparator and its application as current mode ADC, Journal of Electron Devices, 14, 186-1189, 2012.

109. R. Pandey, N. Pandey, B. Sriram, S. K. Paul, Single OTRA Based Analog Multiplier and Its Applications, ISRN Electronics, 2012, Article ID 890615, 7 pages

110. R. Pandey, N. Pandey, B. Sriram, S. K. Paul, Single OTRA Based Analog Multiplier and Its Applications, ISRN Electronics 2012. Article ID 890615, 7 pages

111. R. Pandey, N. Pandey, S. K. Paul Electronically Tunable Transimpedance Instrumentation Amplifier based on OTRA, Journal of Engineering (Hindawi) 2013, Article ID 648540, 5 pages, doi.org/10.1155/2013/648540.

112. K. Gupta, N. Pandey, M. Gupta, MOS Current Mode Logic with Capacitive Coupling, ISRN Electronics, 2012, Article ID 473257, 7 pages, 2012. doi:10.5402/2012/473257.

113. K. Gupta, N. Pandey, M. Gupta, Multi-Threshold MOS Current Mode Logic based Asynchronous Pipeline Circuits, ISRN Electronics 2012, Article ID 529194, 7 pages

114. K. Gupta, N. Pandey, M. Gupta, Low-Power Tri-State Buffer in MOS Current Mode Logic, Analog Integrated Citrcuits and signal processing. April 2013, 75, 1, pp 157-160. **(SCI – 1.337)**

115. R. Pandey, S. Chitransi, N. Pandey, C. Shekhar. Single OTRA based PD Controllers, International Journal of Engineering Science and Technology, 4, 1426-1437, 2012.

116. R. Pandey, N. Pandey, S. K. Paul, A. Singh, B. Sriram, K. Trivedi, Voltage Mode OTRA MOS-C Single Input Multi Output Biquadratic Universal Filter, Advances in Electrical and Electronic Engineering, 10, 337-344, 2012. **Scopus**

117. R. Pandey, N. Pandey, S. K. Paul, Voltage Mode Pulse Width Modulator Using Single Operational Transresistance Amplifier, Journal of Engineering, 2013, Article ID 309124, 6 pages, doi.org/10.1155/2013/309124.

118. R. Pandey, N. Pandey, S. K. Paul, Ajay Singh, B. Sriram, K. Trivedi, Novel grounded inductance simulator using single OTRA, International Journal of Circuit Theory and Application, 42, 10, pages 1069–1079, 2014 **(SCI – 2.038)**

119. N. Pandey, S. K. Paul, SIMO Mixed Mode Universal Filter Journal of Active and Passive Electronic Devices, 7, 215-226, 2012.

120. R. Pandey, N. Pandey, T. Negi, V. Garg, CDBA Based Universal Inverse Filter, ISRN Electronics, 2013, Article ID 181869, 6 pages

121. R. Pandey, N. Pandey, S. K. Paul, K. Anand, K. G. Gautam, Voltage Mode Astable Multivibrator Using Single CDBA, ISRN Electronics, , 2013, Article ID 390160, 8 pages

122. N. Pandey, P. Kumar, Realization of Resistorless Wave Active Filter using Differential Voltage Current Controlled Conveyor Transconductance Amplifier, Radioengineering, 20, 911-916, 2011 **(SCI – 0.925)**

123. N. Pandey, S. K. Paul, Differential Difference Current Conveyor Transconductance Amplifier: A New Analog Building Block for Signal Processing, Journal of Electrical and Computer Engineering, 2011, Article ID 361384, 10 pages **Scopus**

124. N. Pandey, S. K. Paul, Single CDTA-Based Current Mode All-Pass Filter and Its Applications, Journal of Electrical and Computer Engineering 2011, Article ID 897631, 5 pages **Scopus**

125. K. Gupta, R. Sridhar, J. Chaudhary, N. Pandey, M. Gupta, New Low-Power Tristate Circuits in Positive Feedback Source-Coupled Logic, Journal of Electrical and Computer Engineering 2011, Article ID 670508, 6 pages **Scopus**

126. N. Pandey, P. Kumar, Differential voltage current conveyor transconductance amplifier based wave active filter Journal of Electron Devices, 10, 429-432, 2011.

127. N. Pandey, R. Bazaz, R. Manocha MO-CCCCTA-Based Floating Positive and Negative Inductors and Their Applications, Journal of Electrical and Computer Engineering 2011, Article ID 150354, 8 pages, **Scopus**

128. R. Pandey, N. Pandey, S. K. Paul, A. Singh, B. Sriram, K. Trivedi, New Topologies of Lossless Grounded Inductor Using OTRA, Journal of Electrical and Computer Engineering, 2011, Article ID 175130, 6 pages **Scopus**

129. R. Pandey, N. Pandey, M. Bothra, S. K. Paul, Operational Transresistance Amplifier-Based Multiphase Sinusoidal Oscillators, Journal of Electrical and Computer Engineering , 2011. Article ID 586853, 8 pages **Scopus**

130. N. Pandey and S. K Paul, VM and CM Universal Filters Based on single DVCCTA, Active and Passive Electronic Component 2011, Article ID 929507, 7 pages. **Scopus**

131. S. K. Paul, N. Pandey, A novel current mode channel select filter for multi standard wireless receiver, Journal of Active and Passive Electronic Devices, 6 , 327-332, , 2011.

132. K. Gupta, N. Pandey, M. Gupta, A new active shunt-peaked MCML based high performance 1:8 demultiplexer for serial communication, International Journal of Engineering Science and Technology, 2, 4632-4639, 2010.

133. V. Bhatia, N. Pandey and A. Bhattacharyya, Application based comparison of different analog to digital converter architectures, International Journal of Engineering Science and Technology, 2, 3396-3404, 2010.

134. V. Bhatia, N. Pandey and A. Bhattacharyya, A 4-bit expandable current mode ADC based on different current comparator architectures, International Journal of Engineering Science and Technology, 2, 7380-7384, 2010.

135. R. Pandey N. Pandey, R. Anurag, Voltage Reference Circuits: A Classification, International Journal of Engineering Science and Technology, 2, 4929-4935, 2010.

136. N. Pandey, S. K. Paul, A. Bhattachryya, Realization of Generalized Mixed Mode Universal Filter Using CCCIIs, Journal of Active and Passive Electronic Devices, 5, 279 -293, 2010.

137. N. Pandey, S. K. Paul, Digitally Switched Current Mode Universal Filter, Journal of Active and Passive Electronic Devices, 5, 197-208, 2010.

138. N. Pandey, S. K. Paul, SIMO Transadmittance mode Active - C Universal Filter, Circuit and Systems, 1, 54 - 58, 2010.

139. N. Pandey, S. K. Paul, S. B. Jain, Voltage Mode Tow Thomas Universal Filter: A Current Controlled Conveyor Approach, Journal of Active and Passive Electronic Devices, 5, 105 -113, 2010.

140. N. Pandey, S. K. Paul, A. Bhattachryya, Realization of Generalized Mixed Mode Universal Filter Using CCCIIs, Journal of Active and Passive Electronic Devices, 5, 279 -293, 2010.

141. N. Pandey, S. K. Paul and S. B. Jain, A new electronically tunable current mode universal filter using MO-CCCII, Analog Integrated Circuits for Signal Processing, 58, 171-178, 2009. **(SCI – 1.337)**

142. N. Pandey, S. K. Paul, S. B. Jain, New High-Input Impedance Voltage-Mode Universal Biquad: Multi Input Multi Output, Journal of Active and Passive Electronic Devices, 3, 93-100, 2008.

143. N. Pandey, S. K. Paul, S. B. Jain, Voltage Mode Universal Filter using Two Plus Type CCIIs, Journal of Active and Passive Electronic Devices, 3, 165-173, 2008.

144. N. Pandey and S. K. Paul, A Novel Electronically Tunable Sinusoidal Oscillator Based on CCCII(IR), Journal of Active and Passive Electronic Devices, 3, 134-141, 2008.

145. N. Pandey, S. K. Paul, A. Bhattacharyya, S. B. Jain, Insensitive Mixed Mode Biquad Using Reduced Number of Active and Passive Components, Journal of Active and Passive Electronic Devices, 2, 117-125, 2007.

146. N. Pandey, S. K. Paul, Ashok Bhattacharyya and S.B. Jain, A new mixed mode biquad using reduced number of active and passive elements, IEICE Electronics Express, 3, 6, 115-121, 2006. **(SCI- 0.578)**

147. N. Pandey and S. K. Paul, Multi-input Single-output Universal Current Mode Biquad, Journal of Active and Passive Electronic Devices, 1, 229-240, 2006.

148. N. Pandey, S. K. Paul, Ashok Bhattacharyya and S.B. Jain, A novel current controlled current mode universal filter: SITO approach, IEICE Electronics Express, 2, 17, 451-457, 2005. **(SCI- 0.578)**

149. N. Pandey and S. K. Paul, All Pass filter based on CCII- and CCCII-, Int. Journal of Electronics, 91, 485-489, 2004. **(SCI – 1.336)**

International Conference:

1. R. Sivaram, K. Gupta, N. Pandey, Exploration of PFSCL in Subthreshold region of operation for use in ultra-low power applications, 2nd International Conference for Emerging Technology (INCET), May 2021, 1-5.
2. S. Gupta, N. Pandey, RS Gupta, Analog Performance of Dual-Metal Gate Stack Architecture of Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DMGSA-JAM-CSG) MOSFET 2021 Devices for Integrated Circuit (DevIC), 2021, 1-5, doi: 10.1109/DevIC50843.2021.9455896.
3. M. Bansal, P. Semwal, N. Sagar, N. Pandey, Embodying Current division transconductance reduction in M-CDTA and its application as low frequency filter, 2021 3rd International Conference on Signal Processing and Communication, 2021, pp. 360-364, doi: 10.1109/ICSPC51351.2021.9451677.
4. V Garg, V Goel, N. Pandey, A Novel Loadless 6T-SRAM Cell with Isolated Read Port, Journal of Physics: Conference Series 1921 (1), 2021, 012037.
5. G Rajkumar, N. Pandey, New Carry Maskable Adder using Modified Full Swing GDI, Journal of Physics: Conference Series 1921 (1), 2021, 012049.
6. A Jain, N. Pandey, Implementation of Discrete Sine Transform Realization Though Systolic Architecture, In: Nath V., Mandal J.K. (eds) Proceeding of Fifth International Conference on Microelectronics, Computing and Communication Systems. Lecture Notes in Electrical Engineering, vol 748. Springer, Singapore. https://doi.org/10.1007/978-981-16-0275-7_57.
7. S. Gupta, N. Pandey, RS Gupta, Investigation of dual-material double gate junctionless accumulation-mode cylindrical gate all around (DMDG-JLAM-CGAA) MOSFET with High-k gate stack for low power digital applications. *020 IEEE 17th India Council International Conference (INDICON)*, 2020, pp. 1-4, doi: 10.1109/INDICON49873.2020.9342380.
8. A Mann, N Malhotra, A Wadhwa, N. Pandey, Power Gated ECRL Adiabatic Logic Based Optimized Two-Input Multiplexer, 2020 IEEE 17th India Council International Conference (INDICON), 2020, pp. 1-6, doi: 10.1109/INDICON49873.2020.9342133.
9. A. Agarwal, A. K. Trivedi, C. Parashar, N. Pandey, 4-Bit Arithmetic Logic Unit That Uses Adjustable Threshold Pseudo-Dynamic Logic, 2020 7th International Conference on Signal Processing and Integrated Networks (SPIN), 2020, pp. 1105-1109, doi: 10.1109/SPIN48934.2020.9071089.
10. A. S Kumar, A. Wadhwa, N. Pandey, New Adiabatic Error Tolerant Adder I Architectures, 2020 7th International Conference on Signal Processing and Integrated Networks (SPIN), 2020, pp. 240-245, doi: 10.1109/SPIN48934.2020.9070877.
11. V. Bhanoo, A. Gangal, N. Pandey New realization of OFCC Universal TAM filter: A Differentiator based approach, 2020 7th International Conference on Signal Processing and Integrated Networks 504-509

12. S. Garg, S. Goyal, P. Nawale, R Kaur, N. Pandey, Leakage tolerant Wide OR Domino Gate with Modified Keeper Controlling Network, 2019 IEEE 16th India Council International Conference (INDICON), 1-4
13. D. Singh, N. Pandey, Realization of Single CCCDTA based incremental/ decremental type Memconductance Emulator, 2019 International Symposium on Advanced Electrical and Communication Technologies (ISAECT), 1-4
14. P. Sharma, K. Gupta, N. Pandey, A Single-Ended 10-Transistors Static Random Access Memory Bit-Cell with Improved Write-Margins at Low Voltages and High ION-IOFF Ratio, 2019 International Conference on Smart Systems and Inventive Technology, 938-943
15. P. Gangwar, S. Maurya, N. Pandey, Realization of Game Tree Search Algorithms on FPGA: A Comparative Study, 2019 International Conference on Issues and Challenges in Intelligent Computing Techniques (ICICT), 1-3
16. R. Arundeepakvel, P. Khatter, N. Pandey, Realization of Memristor based D-Latch, 2019 International Conference on Computing, Power and Communication Technologies (GUCON), 764-768
17. P. Gangwar, S. Maurya, S Garg, S Goyal, AS Kumar, P Dalmia, N. Pandey, Hardware/Software Co-Design of a High-Speed Othello Solver, 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems 1223-1226
18. P Gangwar, N. Pandey, R. Pandey, Novel Control Unit Design for a High-Speed SHA-3 Architecture, 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems, 904-907
19. B Jha, K. Gupta, N. Pandey, Multiple Threshold CVSL Full Adder Design, 2019 6th International Conference on Computing for Sustainable Global Development (INDIACom) 74-77
20. N Malhotra, A Mann, N. Pandey, Design of Low Power ECRL Based Power Gated 4: 2 Compressor, 2019 6th International Conference on Signal Processing and Integrated Networks (SPIN) 891-895
21. K Chhabra, S Singhal, N. Pandey, Realization of CBTA Based Current Mode Frequency Agile Filter, 2019 6th International Conference on Signal Processing and Integrated Networks (SPIN) 1076-1081
22. V. Bhatia, N. Pandey, SR Prasanthi, Design of an SCL logic based Current Comparator,- 2018 IEEE 61st International Midwest Symposium on circuit and systems, 1134-1137, 2018
23. R. Pandey, N. Pandey, OTRA Based Log and Antilog Amplifiers, 2018 IEEE 61st International Midwest Symposium on circuit and systems, 182-185, 2018.
24. N. Pandey, K. Gupta, B. Choudhary, MCML Dynamic Register Design, 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS), 582-586
25. R Sivaram, K. Gupta, N. Pandey, Low Power Design for Source Coupled Logic Gates, 2018 15th IEEE India Council International Conference (INDICON), 1-5
26. M. Gupta, K. Gupta, N. Pandey, A 32-nm Sub-Threshold 9T SRAM Bit cell with Improved Read and Write performance, 2018 International Conference on Advances in Computing, Communication Control and Networking (ICACCCN) 781-787
27. P. Khatter, N. Pandey, K. Gupta, An Arithmetic and Logical Unit using Reversible Gates 2018 International Conference on Computing, Power and Communication Technologies (GUCON), 476 - 480
28. R. Sivaram, K. Gupta, N. Pandey, New Improved Low Power Triple Tail Cell with Controlled Current Source, 2018 International Conference on Computing, Power and Communication Technologies (GUCON), 462 - 466
29. P Dalmia, A Parashar, A Tomar, N. Pandey, Novel High Speed Vedic Multiplier Proposal Incorporating Adder Based on Quaternary Signed Digit Number System 31st International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems (VLSID), 2018 289-294
30. S. Jain, N. Pandey and K. Gupta, Complete Charge Recovery Diode Free Adiabatic Logic, Fifth International Conference on Signal Processing & Integrated Networks, SPIN 2018.
31. S. Singh, Jatin, N. Pandey and R. Pandey, Precision Capacitance Multiplier with Low Power and High Multiplication Factor, Fifth International Conference on Signal Processing & Integrated Networks, SPIN 2018.

32. D Nand, N. Pandey, R. Pandey and Sunchit Jindal, OFCC based Digitally Controlled Hearing Aid, Fifth International Conference on Signal Processing & Integrated Networks, SPIN 2018.

33. Grover, V Gosain, N. Pandey and K. Gupta Arithmetic Logic Unit Using Diode Free Adiabatic Logic and Selection Unit for Adiabatic Logic Family, Fifth International Conference on Signal Processing & Integrated Networks, SPIN 2018.

34. S. Oruganti, Y Gilhotra, N. Pandey and R. Pandey, New Topologies for OTRA Based Programmable Precision Half-Wave and Full-Wave Rectifiers Multiplier, Recent Developments in Control, Automation and Power Engineering RDCAPE 2017 DOI: 10.1109/RDCAPE.2017.8358291

35. V. Gosain, V. Grover, N. Pandey, K. Gupta, Look ahead carry adder using diode free adiabatic logic family, 2017 2nd International Conference on Telecommunication and Networks (TEL-NET), 2017, 1-4, doi: 10.1109/TEL-NET.2017.8343535.

36. A. Goel, A Gupta, M Kumar, N. Pandey, V. Bhatia Design of 3-Bit Current Mode Flash ADC Using WTA Based Current Comparator, 2017 2nd International Conference on Telecommunication and Networks (TEL-NET), 2017, 1-6, doi: 10.1109/TEL-NET.2017.8343531

37. A Gupta, A. Goel, M Kumar and N. Pandey, Novel Architecture for Area and Delay efficient Vedic Multiplier, Recent Developments in Control, Automation and Power Engineering RDCAPE 2017, 45-48, doi: 10.1109/RDCAPE.2017.8358237

38. R. Joshi, A. Raghuvanshi, Y. Gilhotra, S. Sharma, S. Sharma, P. Dalmia, N. Pandey, An FPGA based floating point Gauss-Seidel iterative solver, 2017 14th IEEE India Council International Conference (INDICON), 2017, 1-6, doi: 10.1109/INDICON.2017.8487543

39. P. Dalmia, A. Parashar, G. Aggarwal, R. Dang, N. Pandey, Fast Combinational Architecture for a Vedic Divider, 2017 14th IEEE India Council International Conference (INDICON), 2017,1-5, doi: 10.1109/INDICON.2017.8487598.

40. G. Komanapalli, N. Pandey, R. Pandey, OTRA based second and third order sinusoidal oscillators and their phase noise performance, AIP Conference Proceedings 1859 (1), 020017, 2017

41. D Nand, N. Pandey, R. Pandey, P Tripathi, P Gola, OFCC based voltage and transadmittance mode instrumentation amplifier AIP Conference Proceedings 1859 (1), 020109, 2017

42. R K Agrawal, N. Pandey, K. Gupta Implementation of PFSCL razor flipflop, 2017 International Conference on Computing Methodologies and Communication (ICCMC), 6-11, 2017

43. N. Saxena, S. Dutta, N. Pandey, K. Gupta, Implementation and Performance Comparison of a Four-Bit Ripple-Carry Adder Using Different MOS Current Mode Logic Topologies, International Conference on Computational Science and Its Applications, 299-313, 2017

44. Y. Nigam, R. Pandey, N. Pandey, Curvature compensated TIA based BGR, 4th International Conference on Signal Processing and Integrated Networks (SPIN), 206-209, 2017

45. S. Gupta, K. Gupta, N. Pandey, Stability analysis of different dual-port SRAM cells in deep submicron region using N-Curve Method International Conference on Signal Processing and Communication (ICSC), 431-436, 2016

46. D. Sachan, D. Nand, N. Pandey, Universal biquadratic filter using Operational Floating Current Conveyor (OFCC), Microelectronics (ICM), 2016 28th International Conference on, 317-320, 317-320

47. K. Gupta, P. Shukla, N. Pandey, On the implementation of PFSCL adders Second International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH), 287-291, 2016

48. V. Bhatia, N. Pandey, A Novel Ultra Low Power Current Comparator, International Conference on Advances in Computing and Data Sciences, 423-432, 2011

49. S. Kareer, A. Kumar, K. Gupta, N. Pandey, A Novel Bulk Drain Connected 6T SRAM Cell, International Conference on Advances in Computing and Data Sciences, 232-242, 2016

50. G. Singh, A. Gupta, K. Gupta, N. Pandey, FPGA implementation of different NRZ line coding schemes, Information Processing (IICIP), 2016 1st India International Conference on, 1-7

51. V. V. Kumar, C. Malhotra, V. K. Ahalawat, N. Pandey, R. Pandey, Voltage and Current Mode OFCC Based Semi Gaussian Shapers, 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), 10.1109/ICPEICES.2016.7853446

52. P. Tripathi, P. Gola, P. Pahalwan, N. Pandey, R. Pandey, Design of Digitally Controlled OTRA based Filter for Hearing Aid Application, 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES) doi: 10.1109/ICPEICES.2016.7853468.

53. K. Gupta, S. Bagga, N. Pandey, Efficient CVSL based Full Adder Realizations, 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), doi: 10.1109/ICPEICES.2016.7853544

54. A. Goel, R. Pandey, N. Pandey, S. Yadav, Operation Trans-resistance Amplifier based low-voltage reference, 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), doi: 10.1109/ICPEICES.2016.7853474

55. C. Malhotra, V. K. Ahalawat, V. V. Kumar, R. Pandey, N. Pandey, Voltage differencing buffered amplifier based quadrature oscillator, 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), doi: 10.1109/ICPEICES.2016.7853457.

56. V. Bhatia, K. Gupta, N. Batra, N. Pandey, Modelling a Simple Current to Voltage Converter using Artificial Neural Networks, 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), 1-4, doi: 10.1109/ICPEICES.2016.7853224.

57. A. Jain, N. Pandey, R. Pandey, Realization of frequency-hopping filters using CDTA and VDTA, 3rd International Conference on signal processing and integrated networks, 2016

58. N. Saxena, S. Dutta, N. Pandey, K. Gupta, Implementation of Asynchronous Pipeline using Transmission Gate logic, 2016 International Conference on Computational Techniques in Information and Communication Technologies (ICCTICT), 101-106, doi: 10.1109/ICCTICT.2016.7514560.

59. K. Gupta, U Mittal, R Baghla, N. Pandey, Implementation of PFSCL Demultiplexer, 2016 International Conference on Computational Techniques in Information and Communication Technologies (ICCTICT), 490-494, doi: 10.1109/ICCTICT.2016.7514630.

60. A. Tyagi, N. Pandey, K. Gupta, PFSCL based Linear Feedback Shift Register, 2016 International Conference on Computational Techniques in Information and Communication Technologies (ICCTICT), 580-585, doi: 10.1109/ICCTICT.2016.7514646.

61. N. Pandey, Nitish, K. Gupta, T Kuhar, Pre-scalar for Diode Free Adiabatic Logic Family, 2016 International Conference on Computational Techniques in Information and Communication Technologies (ICCTICT), DOI: 10.1109/ICCTICT.2016.7514628.

62. R. Pal, R. C. Tiwari, N. Pandey, R. Pandey, Pulse Width Modulator using CDBA based relaxation oscillator, IEEE International Conference ICIIS-2014. DOI 10.1109/ICIINFS.2014.7036564

63. R. Ranjan, R. Pandey, N. Pandey, G. Singh Linear Phase Detector Using OTRA IEEE International Conference SPIN-2015. 917-920, doi: 10.1109/SPIN.2015.7095328.

64. R. Pandey, N. Pandey, G. Komanapalli, A. K. Singh, R. Anurag, New realizations of OTRA based sinusoidal oscillator, 2015 2nd International Conference on Signal Processing and Integrated Networks (SPIN), 2015, 913-916, doi: 10.1109/SPIN.2015.7095323.

65. N. Pandey, P. Tripathi, R. Pandey, R. Batra, OFCC based Logarithmic Amplifier, 2014 International Conference on Signal Processing and Integrated Networks (SPIN), 2014, 522-525, doi: 10.1109/SPIN.2014.6777009.

66. N. Pandey, N. Dadhich, Mohd. Z. Talha, Realization of 2:4 reversible decoder and its applications, 2014 International Conference on Signal Processing and Integrated Networks (SPIN), 2014, 349 – 353, 2014. DOI: 10.1109/SPIN.2014.6776976

67. Himanshu Puri, Kshitij Ghai, K. Gupta, N. Pandey A Novel DFAL based Frequency Divider, 2014 International Conference on Signal Processing and Integrated Networks (SPIN), 2014, 526-530, doi: 10.1109/SPIN.2014.6777010.

68. Radhika, N. Pandey, K. Gupta, M. Gupta, Low Power D-latch design using MCML Tri-state Buffers, International Conference on Signal Processing & Integrated Networks, 531-535. 2014. DOI: 10.1109/SPIN.2014.6777011.

69. K. Gupta, N. Pandey and M. Gupta, Performance Improvement of PFSCL gates through Capacitive Coupling, International Conference on Multimedia Signal Processing and Communication Technologies (IMPACT-2013) DOI: 10.1109/MSPCT.2013.6782115.

70. K. Gupta, R. Tanwar, N. Pandey and M. Gupta, A Novel High Speed MCML Square Root Carry Select Adder for Mixed-Signal Applications, International Conference on Multimedia Signal Processing and Communication Technologies (IMPACT-2013) DOI: 10.1109/MSPCT.2013.6782117

71. V. Bhatia, Mohini Madaan, Baljeet Kaur, N. Pandey and A. Bhattacharyya, A Novel CC-II Based Current Comparator And Its Application In a Current Mode Flash ADC, International Conference on Multimedia Signal Processing and Communication Technologies IMPACT-2013, 2013, 217-222, doi: 10.1109/MSPCT.2013.6782122.

72. Garima Varshney, N. Pandey, R. Pandey, A. Bhattachayya, Performance Comparison Of Filter Circuits Based On Two Different Current Conveyor Topologies, 2013 INTERNATIONAL CONFERENCE ON SIGNAL PROCESSING AND COMMUNICATION (ICSC), 2013, 419-423, doi: 10.1109/ICSPCom.2013.6719825.

73. N. Pandey, S. Sayal and R. Pandey, CDTA Based Semi Gaussian Shapers for Detector Readout Front Ends, 2013 International Conference on Circuits, Power and Computing Technologies (ICCPCT), 2013, 703-708, doi: 10.1109/ICCPCT.2013.6528962.

74. N. Pandey, S. Sayal and R. Pandey, DDCCTA Based Semi Gaussian Shapers for Detector Readout Front Ends, IEEE International Conference on Circuit, Power and Computing Technologies, (ICCPCT), 2013, 709-714, doi: 10.1109/ICCPCT.2013.6528963.

75. N. Pandey, R. Pandey, S.K. Paul, Novel single input five output voltage mode universal filter based on DDCCTA, International Conference on Computer and Communication Technology (ICCCT-2012), Allahabad,

76. N. Pandey, Sakshi Arora, Rinku Takkar, Realization of DVCCCTA Based Mutually Coupled Circuit, International Conference on Computer and Communication Technology (ICCCT-2012), Allahabad.

77. R. Pandey, N. Pandey, S. K. Paul, Mandeep Singh, Manish Jain, Voltage Mode single OTRA based Biquadratic Filters, International Conference on Communication and Computer Technology, ICCCT-12, pp, 63 – 67, Nov. 2012.

78. R. Pandey, N. Pandey, S. K. Paul, MOS-C Third Order Quadrature Oscillator using OTRA, Third International Conference on Communication and Computer Technology, ICCCT-12, 77 -80, Nov. 2012.

79. R. Pandey, N. Pandey, S. K. Paul, Mandeep Singh, Manish Jain, Voltage Mode Biquadratic Filter using Single OTRA, Fifth India International Conference on Power Electronics, IICPE-2012, 1 - 4, Dec. 2012.

80. R. Sridhar, N. Pandey, V. Bhatia, A. Bhattacharyya, On improving the performance of traff's comparator, Fifth India International Conference on Power Electronics, IICPE-2012, Dec. 2012.

81. K. Gupta, N. Pandey, M. Gupta, Low Power Multi-Threshold MOS Current Mode Logic Asynchronous Pipeline Circuits, Fifth India International Conference on Power Electronics, IICPE-2012, Dec. 2012.

82. Arun Rudra, N. Pandey, S. Indu, Evolutionary algorithm based combinational circuit design, Fifth India International Conference on Power Electronics, IICPE-2012, Dec. 2012

83. V. Bhatia, N. Pandey, A. Bhattacharyya, An expandable current-mode ADC with power optimization technique, Proceedings of IEEE 2012 1st International Conference on Recent Advances in Information Technology (RAIT), Digital Object Identifier: 10.1109/RAIT.2012.6194551, Publication Year: 2012 , Page(s): 765 – 770.

84. P. Iswerya, S. Gupta, M. Goel, V. Bhatia, N. Pandey, A. Bhattacharyya, Delay area efficient low voltage FVF based current comparator, Proceedings of IEEE 2012 1st Students Conference on Engineering and Systems (SCES), Digital Object Identifier: 10.1109/SCES.2012.6199088.

85. V. Bhatia, N. Pandey. A. Bhattacharyya, Low power delay proficient current mode ADC design, Proceedings of IEEE International Conference on Power, Control and Embedded Systems (ICPCES 2012).

86. K. Gupta, R. Sridhar, Jaya Chaudhary, N. Pandey, M. Gupta Performance Comparison of MCML and PFSCL Gates in 0.18 µm CMOS Technology International Conference on Computer and Communication Technology (ICCCT-2011), Allahabad, 230 – 233

87. N. Pandey, Sahil Kapur, Pushkar Arora, S. Malhotra, MO-CCCCTA based PID controller employing grounded passive elements International Conference on Computer and Communication Technology (ICCCT-2011) , Allahabad, 270 – 273

88. N. Pandey, Sahil Kapur, Pushkar Arora, S. Malhotra Novel Voltage Mode Multifunction Filter based on Current Conveyor Transconductance Amplifier, Proc. of Int. Conf. on Advances in Electrical & Electronics 2010 89 – 92

89. N. Pandey, Sahil Kapur, Pushkar Arora, S. Malhotra First order voltage mode MO-CCCCTA based All Pass filter, Proc. of 2011 International Conference on Communications and Signal Processing (ICCSP), 535 -537.

90. N. Pandey R. Bazaz R. Manocha, Active RLC ladder filter simulation using newly proposed CCCCTA block, Proc. of 2011 International Conference on Communications and Signal Processing (ICCSP), 554-557

91. N. Pandey, S. K. Paul, A. Bhattacharyya, A Novel Electronically Tunable Filter for Multi Standard Wireless Receiver, Proc. of International Conference on Computer and Communication Technology (ICCCT-2010) , September 17-19, 2010, MNNIT, Allahabad, 282 – 284

92. K. Gupta, N. Pandey, M. Gupta, A Novel Active Shunt-Peaked MCML-based High Speed Four-Bit Ripple-Carry Adder, Proc. Of International Conference on Computer and Communication Technology (ICCCT-2010), September 17-19, 2010, MNNIT, Allahabad. 285 – 289

93. R. Pandey, N. Pandey, Rajendra Kumar,and Garima Solanki A Novel OTRA Based Oscillator with Non Interactive Control, Proc. of International conference on Communication and Computer Technolgy, ICCCT'10,Allahabad.p 658 – 660

94. K. Gupta, N. Pandey, M. Gupta, Shunt-Peaking in MCML Memory Element Design in 0.18µm CMOS Technology, Proc. of 2010 Annual IEEE India Conference (INDICON), 1-4

95. V. Bhatia, N. Pandey and A. Bhattacharyya, A 4-bit Expandable Algorithmic current-Mode Analog to Digital Converter for use in Digital Control Systems, Proc. of India International Conference on Power Electronics 2010, p.1 – 5

96. N. Pandey, S. K. Paul, Analog Filters based on 0.25 µm CMOS Differential Voltage Current Conveyor Transconductance Amplifier(DVCCTA), Proc. of India International Conference on Power Electronics 2010, p. 1 – 4

97. S. K. Paul, N. Pandey, A. Bhattacharyya, Current Controlled Conveyor based Transadmittance mode Universal Filter Proc. IEEE Symposium on Industrial Electronics and Applications (ISIEA2009) Malaysia, 264-267.

98. N. Pandey, S. K. Paul, A. Bhattacharyya, CMOS Channel Select Filter For Multi Standard Wireless Receiver, International Conference on Innovative Technologies (ICIT-09): Research and Development in Science, Technology and Management.

99. K. Gupta, N. Pandey, M. Gupta, Low power Active Shunt-Peaked MCML-based Circuits for Mobile Applications in GHz range International Conference on Innovative Technologies (ICIT-09): Research and Development in Science, Technology and Management.

100. S. K. Paul, N. Pandey, S. B. Jain, Realization of Plus-Type CCCIIs Based Voltage, Proc. IEEE International Symposium on Integrated Circuits (ISIC-2007), 119 – 122.

101. S. K. Paul, N. Pandey, S. B. Jain, Digitally Controlled Current Mode Universal Filter, Proc. IEEE International Symposium on Integrated Circuits (ISIC-2007), 572 – 575.

102. N. Pandey, S. K. Paul, S. B. Jain, A novel current mode channel select filter for Multi standard wireless receiver, accepted in IEEE region 10 conference to be held in Hyderabad during Nov. 2008.

103. N. Pandey, S. K. Paul, S. B. Jain, A. Bhattacharyya, Electronically Tunable Current Mode Universal Filter: MIMO Approach, Proc. 3rd International Conference on Computers and Devices for Communication (CODEC-06), 170 – 173.

104. N. Pandey, S. K. Paul, A. Bhattacharyya, S. B. Jain, Voltage Mode Tow Thomas Universal Filter: A Current Controlled Conveyor Approach, Proceedings of General Assembly of International Union of Radio Sciences held in Delhi from Oct. 23-29, 2005.

105. N. Pandey, S. K. Paul, A. Bhattacharyya, An insensitive current mode universal biquad: multi-input multi-output, Proceedings of IEEE International Symposium on Circuits and Systems held in Kobe, Japan, 3399-3902, 2005.

106. N. Pandey, S. K. Paul, Realization of current mode multifunction filter using translinear conveyor, Proceedings of International Conference on Computers and Devices for Communication, Kolkata, Jan 1-3, 2004.

107. N. Pandey, S. K. Paul, Realization of Tow Thomas Biquad Using Translinear Current Conveyors, Proceedings of International Conference on Communication, Device and Intelligent Systems, Kolkata, 243-246, Jan 8-10, 2004.

National Conference:

1. N. Pandey, S. K. Paul, A. Bhattacharyya, Single CCII- and CCCII-based all pass filters- New generic configurations, International Conference on Electronic and Photonic Materials, Devices and Systems – 2006

2. N. Pandey and S. K. Paul, All pass filter based on CCCII with negative intrinsic resistance, Horizon of Telecommunications held in Calcutta from Feb. 3 – 5, 2003.

3. N. Pandey and S. K. Paul, All pass filter based on CCII and CCCII, National Conference on Microchip Design and Technology held in Maharaja Surajmal Institute of Technology, Delhi from Mar. 6-8, 2003.

4. I. J. Kumar and N. Pandey, Fuzzy logic approach to cryptosystem synthesis, National Conference on Information Security held in Bharati Vidyapeeth's College of Engineering from Jan. 8-9, 2003.

5. V. Bhatia, N. Pandey and H. M. Rai, Improving Signal Processing with ADCs based on current mode algorithm, in National Seminar on Cutting edge technologies in electronic communication held in Sant Longowal Institute of Technology Mar. 14, 2004.

6. N. Pandey and V. Bhatia, Improving Signal Processing with ADCs : A current mode approach, in National Conference on VLSI Design and Technology held in Bharati Vidyapeeth's College of Engineering from Apr. 15-16, 2004.

7. N. Pandey, S. K. Paul, A. Bhattacharyya , A Novel Electronically Tunable Filter for Multi Standard Wireless Receiver, Proceedings of IETE Mid Term Symposium 2005, 179-184