The **Digital System Architecture and Design (DSAD)** research Group at the Department of Electronics and Communications Engineering at Delhi Technological University, led by Prof. Dr. Neeta Pandey, focuses on the frontend design of digital hardware for solving challenging real-world problems. The research is primarily focused on the implementation of digital systems targeting the most recent advances in Computation, Information Security, and Artificial Intelligence as well as the optimization and enhancement of existing hardware architectures.

The primary goal of this group is to develop a research temperament among students and provide them with a platform to hone their skills in digital frontend design under capable mentorship. The research done by this group has been acknowledged by reputed International conferences, which bears testimony to the dedication and commitment of the members to achieve this goal.

People:

Faculty Advisor: Prof. Dr. Neeta Pandey

Student Advisor: Preyesh Dalmia (Presently at Synopsys)

Past Members:

1. Abhinav Parashar (Presently at Texas Instruments)
2. Akshi Tomar (Presently at Texas Instruments)
3. Aman Raghuvanshi (Presently at Qualcomm)
4. Ramakant Joshi (Presently at Samsung Semiconductor India R&D)
5. Vikas (Presently at Samsung Semiconductor India R&D)

Current Members:

- Final Year:
    1. Gaurav Aggarwal
    2. Pranav Gangwar
    3. Radhika Dang
    4. Satvik Maurya
    5. Shivani Sharma
    6. Suyash Sharma
    7. Yatin Gilhotra
- Pre – Final Year:
    1. Aditya S. Kumar
    2. Prabhakar Nawale
    3. Rattan Kaur
    4. Sagar Jain
    5. Sakshi Goyal
    6. Shubham Garg

Publications:

1. Novel High-speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system: This paper presents a high-speed Vedic multiplier based on the Urdhva Tiryagbhyam sutra of Vedic mathematics that incorporates a novel adder based on Quaternary Signed digit number system. Three operations are inherent in multiplication: partial products generation, partial products reduction, and addition. A fast adder architecture therefore greatly

enhances the speed of the overall process. A Quaternary logic adder architecture is proposed that works on a hybrid of binary and quaternary number systems. A given binary string is first divided into quaternary digits of 2 bits each followed by parallel addition reducing the carry propagation delay. The design doesn't require a radix conversion module as the sum is directly generated in binary using the novel concept of an adjusting bit. The proposed multiplier design is compared with a Vedic multiplier based on multi voltage or multi value logic [MVL], Vedic Multiplier that incorporates a QSD adder with a conversion module for quaternary to binary conversion, Vedic multiplier that uses Carry Select Adder and a commonly used fast multiplication mechanism such as Booth multiplier. All these designs have been developed using Verilog HDL and synthesized by Synopsys Design Compiler. They have been realized using the open source NAN gate 15nm technology library. The proposal shows a maximum of 88.75% speed improvement with respect to Multi Value logic based 128x128 Vedic multiplier while the minimum is 17.47%. (**In Press; P. Dalmia, Vikas, A. Parashar, A. Tomar, N. Pandey, "Novel High-speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system", 31st International Conference on VLSI Design, 2018**)

2. An FPGA based floating point Gauss-Seidel iterative solver: In this paper, an FPGA-based single precision floating point hybrid iterative architecture for solving a linear system of equations is proposed. The novel architecture implements Gauss-Seidel method using a Jacobi method based building block. The design takes advantage of the fast convergence of Gauss-Seidel Method conflated with parallel, pipelined architecture of Jacobi Iterative solver resulting in a much efficient architecture with acceptable hardware augmentation. The whole design has been implemented in Verilog HDL, having Virtex 7 XCV2000T as targeted device. Other design optimizations include using modified high-speed radix 4 multiplier and optimized high-speed 2's complementer. The efficacy of the design is tested and implemented in solving nonsingular, exactly determined and strictly diagonally dominant coefficient matrix based dense and sparse linear system of equations with different number of variables. The design results in reduced number of iterations and equivalent speedups are presented, which are calculated factoring in, the increased delay effects. (**In Press; R. Joshi, A. Raghuvanshi, Y. Gilhotra, S. Sharma, S. Sharma, P. Dalmia, N. Pandey, "An FPGA based floating point Gauss-Seidel iterative solver", 14th IEEE INDICON, 2017**)

3. Fast Combinational Architecture for a Vedic Divider: This paper proposes a fast, purely combinational implementation of a divider, based on the Dhwajanka Sutra of Vedic mathematics. Vedic mathematics offers algorithms that are computationally efficient over conventional arithmetic algorithms. Dhwajanka Sutra has been chosen as it is an algorithm efficient for all possible cases, unlike other sutras for division (Nikhilam and Paravartya) which are case specific. The simplicity of the Vedic algorithm implemented in combinational form has reduced computation time significantly. The proposed design is compared with existing divider architectures implemented on an FPGA namely Non-restoring Algorithm based Divider, Vedic Divider (Paravartya Algorithm), Vedic Divider (Nikhilam Algorithm), Decimal Divider based on Newton Raphson algorithm, Decimal Divider based on SRT algorithm and Combination divider algorithms. The proposed vedic divider shows a maximum of 273.72% speed improvement while the minimum is 99.95%. The results have been validated using the Xilinx ISE Design Suite 14.7, on the Virtex5 (xc5vlx20T-2ff323) FPGA Target Technology and the design has been implemented in Verilog. (**In Press; P. Dalmia, A. Parashar, G. Aggarwal, R. Dang, N. Pandey, "Fast Combinational Architecture for a Vedic Divider", 14th IEEE INDICON, 2017)**

Completed Projects:

1. Area efficient architecture for Elliptic Curve Cryptography Coprocessor.
2. FPGA based Tic-Tac-Toe Solver using Game Theory.

Current Projects:

1. HW/SW co-design of an Othello solver on Xilinx's Zynq Soc 7000
2. FPGA based speech recognition system using machine learning.
3. Implementation of a High-Performance GPU ALU.

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