IEEE Blended Learning Program online series on VLSI

IEEE, the world's largest technical professional association, is dedicated to advancing technology for the benefit of humanity.

IEEE-Blended Learning program is an initiative from IEEE that has been specifically designed for the circuit branch students. It offers industry-oriented courses in and bridges the gap between academics and the needs of the Industry. Students at Delhi Technological University are already learning IEEE-BLP VLSI courses, these VLSI courses are short term skills enhancement certificate courses.

In addition to the ELearning courses IEEE-BLP is also offering Virtual online sessions on VLSI so that students at Delhi Technological University can get a holistic learning experience and get enhanced knowledge on the VLSI subject.

VLSI online Series:

In this VLSI lecture series, we are organising 4 online sessions on key VLSI topics such as ASIC Design, Logic Design, RTL Design and RTL verification using Verilog. Along with covering the overview of the topics these sessions will also cover case studies, demos, and examples which will help learner gain practical knowledge of the Subject. These sessions can be joined over Webex, the details of the Sessions are as follows:

Please register for all 4 sessions, Registration link has been provided along with each session.

1st Session: Sep 12th 3:30pm to 5:00pm

Registration Link for Session 1:
https://ieee.webex.com/ieee/onstage/g.php?MTID=e5c96567951e0b4ddbcbcec905e7a7f6d

Topic: ASIC Design Flow

- Overview of Industry, types, challenges
- Overview of the ASIC Flow
- Case Study - Demos in this case

2nd Session: Sep 19th 3:30pm to 5:00pm

Registration Link for Session 2:
https://ieee.webex.com/ieee/onstage/g.php?MTID=ee7bd04e70cf4f40508640056d8e87f3e

Topic: Logic Design

- Overview of Logic Design with focus on BA, Combo and Seq
- Overview of Sequential design and FSM
- Case Study - Explain a EVM in details

3rd Session: Sep 26th 3:30pm to 5:00pm

Registration Link for Session 3:
https://ieee.webex.com/ieee/onstage/g.php?MTID=e96217a5c055bbfe55c45f29afc2fa651

Topic: RTL Design

- Overview of RTL Design Flow
- Types of Verilog commands and coding guidelines
- Case Study - Explain a FIFO, I2C using a tool

4th Session: October 3rd 3:30pm to 5:00pm

Registration Link for Session 4:
https://ieee.webex.com/ieee/onstage/g.php?MTID=e0f114edc08e4b803506b3a10387a97b2

Topic: RTL Verification using Verilog

- Overview of RTL Verification Flow
- Overview of a Verification test bench
- Case Study - Verify a FIFO using a tool

How to Register:

1) Please click on the respective link > It will open-up the registration page > Please click on "register" in event status

2) Register by Entering the following:

3) On the day of the event join the event by clicking on the link as received in the mail